Docket # 68996

METHOD AND APPARATUS FOR INTERFACING A SPECTRUM DIGITAL INCORPORATED TMS470 EVALUATION BOARD WITH A SPECTRUM DIGITAL INCORPORATED TMS320LC54X EVALUATION BOARD

FIELD OF THE INVENTION

The present invention relates in general to an interface between first and second processor emulating evaluation boards, and more specifically to a bridge board between a TMS470 processor evaluation module and a TMS320C54XX processor evaluation module.

BACKGROUND OF THE INVENTION

Integrated circuits (IC) are well known in the field of electronics and often incorporate millions of individual electronic components onto a single substrate. Designing such IC's with their millions of components and the corresponding millions of connections, can be very time consuming and expensive, as well as the testing of a new design. Therefore it is desirable to reuse existing designs, or portions of existing designs, when designing a new IC.

Different types of circuits have been designed for IC's, which perform a general function. An example of these different types of circuits, are processors, memory devices, programmable logic devices (PLD) and analogue to digital convertors (A/D). These types of circuits are further subdivided into subtypes with different features. The different types of circuits are often formed into individual IC's, mounted on a printed circuit board and connected to each other for a specific application.

More recently, Application Specific Integrated Circuits (ASIC) are being designed where a single substrate contains several different types of circuits in a particular combination which has been designed for a specific application. Existing designs for the different types of circuits are combined into one integrated circuit to make the ASIC. In this way, only the design and testing of the connections between the known types of circuits is necessary, and not the design and testing of all of the individual components of an integrated circuit.

SUMMARY AND OBJECTS OF THE INVENTION

It is a primary object of the present invention to provide an arrangement which emulates the connection between known types of circuits on an integrated circuit, especially between two

known types of processor circuits formed into a single integrated circuit.

The present invention particular addresses the problem of emulating the connection between a general purpose processor such as the TMS470 also known as an ARM RISC (Reduced Instruction Set Computer) processor, and a Digital Signal Processor (DSP) such as the Texas Instruments C549DSPs. In telephone equipment, it is very desirable to combine these two processors, or two processors that are similar. These two processors are also combined with other components for applications in a telephone system.

The computer program or computer code that runs on these processors is specifically designed for the application where the ASIC will be used, and for the particular processor that will be incorporated onto the ASIC. Creating an ASIC involves very high initial costs. Masks or templates need to be created with very complicated and small dimensions. Therefore it is desirable to test an ASIC design very thoroughly before expending the effort to create the masks or templates for the actual ASIC. Creating the design and the actual manufacture can take long periods of time. The processors on the ASIC need software and it is desirable to begin creating and testing the software before the actual ASIC is created.

One way to test a proposed ASIC design, and begin creating and testing software for the ASIC, is to simulate the ASIC through a model. Since similar processor designs are used over and over again in ASICs, evaluation boards or emulators have been created to simulate or model the operation of specific processors in an ASIC. An example of these evaluation boards is the Spectrum Digital Incorporated TMS470 evaluation board and the Spectrum Digital Incorporated TMS320LC54X evaluation board. These boards are designed to be

connected to a computer workstation where the workstation runs software which emulates the operation of the respective processor in an ASIC. Details of these evaluation modules or boards can be found in the technical reference documents attached as an appendix to this specification and incorporated by reference.

Occasionally two processors are incorporated into one ASIC. Each processor has its own software and in actual operation, the processors communicate with each other to operate on the data. As described above, evaluation boards are available for the individual processors, TMS320 and the TMS470. With these evaluation boards, the respective portions of the ASIC can be tested separately and software can be developed and tested for the respective processors independently. Each of the evaluation modules connect to a software emulator cable in order to operate. A person therefore developing and testing software for an ASIC with two processors must therefore have data transfers between processors go through the two emulator cables and the workstation.

The TMS470 evaluation board has two connectors labeled JP1 and JP2. These connectors connect to data lines, address lines and control lines of the TMS470 evaluation board, and these lines correspond to actual data lines, address lines and control lines of the processor when it is incorporated onto an ASIC. The TMS320 evaluation module also has data lines, address lines and control lines which correspond to actual data lines, address lines and control lines on the actual processor incorporated onto the ASIC.

The present invention connects the two evaluation modules with a bridge board that converts signals from one module into signals that the other module can read. The bridge board

performs translation of signal formats on both of the boards and also synchronizes the signal formats on both boards so that both boards are able to operate together.

With this bridge board, and its specific connections to both of the evaluation modules, a single workstation, preferably connected to the TMS470 module is able to not only control the TMS470 module but also the TMS320 module. Software for the TMS320 can be loaded from the workstation through the TMS470 module, through the bridge board and into the TMS320 module. The software in both of the evaluation modules can then operate and interact with each other through the bridge board. A single workstation is thus able to develop and test software for two processors on an ASIC, and the single workstation is also able to test how the software for two processors interacts. The single workstation controlling both evaluation modules and being able to test the software for the individual modules both individually and together, allows the development and testing of the software for a dual processor ASIC to start earlier and greatly reduces the time and effort needed to develop and test the software.

The various features of novelty which characterize the invention are pointed out with particularity in the claims annexed to and forming a part of this disclosure. For a better understanding of the invention, its operating advantages and specific objects attained by its uses, reference is made to the accompanying drawings and descriptive matter in which a preferred embodiment of the invention is illustrated.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

Fig. 1 is a schematic diagram of the emulating arrangement using a bridge board to translate and synchronize between two processor evaluation modules;

Fig. 2 is a schematic diagram of the logic components and connections on the bridge board;

Fig. 3 is a flow chart of the operations performed in the bridge board for converting the signals between the two processor evaluation modules;

Fig. 4 is a state diagram of the operations performed in the bridge board for converting the signals between the two processor evaluation modules;

Fig. 5 is a schematic diagram of the connection between the signal lines of the TMS470 module and the JP1 and JP2 connectors;

Fig. 6 is a schematic view of the data lines, signal lines and control lines of the TMS320 processor evaluation module.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to the drawings, in particular to Fig. 1, a workstation 1 is connected to a TMS470 processor evaluation module 3 by a software emulator cable 5. The cable 5 connects to the TMS470 module 3 at a Jtag connector 7 on the module 3. Also on the TMS470 module 3, are connectors JP1 and JP2. These connectors connect to signal lines of the TMS470 module 3 as shown in Fig. 5. The workstation 1 is able to control the TMS470 module so that software developed for the actual TMS470 processor on the ASIC can be executed, controlled and monitored. A description of the TMS470 processor evaluation module 3 is enclosed in the appendix. Using a TMS470 processor evaluation model 3 with a workstation to develop and

test software for TMS470 processor it is well known to those of ordinary skill in the art and therefore no further explanation of the TMS470 processor evaluation module, or its operation is necessary.

A TMS320 processor evaluation module 9 is also provided. This TMS320 module also has a Jtag connector 11 on the module 9 for connection to an emulator cable and then to a workstation. However, according to the present invention, no separate emulator cable for the TMS320 evaluation module 9 is needed. Details of the TMS320 processor evaluation module are described in the technical reference manual enclosed in the appendix of this application. Operation of the TMS320 module 9 is well known to those of ordinary skill in the field of the present invention. Therefore no further description of unrelated module details, or the operation, of the TMS320 module are necessary.

The TMS320 processor evaluation model 9 has data lines, address lines and control lines as shown in Fig. 6. The TMS320 processor is also known as a digital signal processor (DSP).

The present invention places the header portion of a connector on the TMS320 processor module 9. This allows a TMS320 cable 13 to be connected to the data lines, address lines and control lines of the Host Port Interface (HPI) of the TMS320 module 9 as shown in figure 6.

The bridge board 15 has a connector P1 which attaches to the TMS320 cable 13. Fig. 2 shows the connector P1 and the signals which connector P1 receives from the TMS320 module 9 over the TMS320 cable 13. The TMS320 cable 13 is preferably a 34 pin ribbon cable. The TMS470 cable 17 has connector ends for connecting to double row 1.27 connectors

with 60 pins each. The bridge board 15 also has connectors JP1 and JP2 which connect via TMS470 cables 17 to the respective connectors JP1 and JP2 of the TMS470 module 3. In an alternative, the bridge board 15 could directly connect to the TMS470 module 3 without any cables in a "sandwich" fashion. The connectors in one board pop directly to the ones in the other board.

In the preferred embodiment, the TMS320 cable connects to the TMS320 module signal lines that are associated with a host port interface (HPI) and is part of the actual TMS320 processor on an ASIC. The signal line connections used by the bridge board 15 on the TMS470 module 3 and the TMS320 module 9 are typically used to monitor status of the individual lines of the processors during operation of different ASIC software programs running on the respective modules.

The bridge board 15 includes a Programmable Logic Device (PLD), preferably an Altera PLD of the MAX 7000 device family, model EPM7128SLC84-6 and the June 1996 ver. 4., the data sheet of which is attached in the appendix.

The PLD is connected to the JP1, JP2 and P1 connectors as shown in Fig. 2. The PLD runs its own software program which translates signals from the TMS470 module 3 into a format that can be used by the TMS320 module 9, and vice versa. The program uses the control signals and the address signals from each board to detect when one board has data to transfer to another board, and when each board is able to receive data, and when to indicate to a board that there is data to be received. An example of a software program for the Altera CPLD is enclosed in the appendix with the title "ARM_HPI". By the bridge board 15 being

connected to the TMS470 processor module 3 and the TMS320 processor module 9, software engineers can begin the code development for an ASIC before the ASIC is actually created or, even possibly before the design is completely finished. The software engineers can include software code for the TMS470 module that will also control the TMS320 module by writing to the HPI port of the TMS320 module 9 through the bridge board 15. Only one software cable 5 is now needed to be connected to the TMS470 module 3 instead of separate cables for each of the modules 3 and 9. This provides the software engineers with a software environment that is very similar to the finished ASIC and allows the software engineers to start the software development at an early stage.

During operation of the invention, the PLD and software program will be enabled when the TMS470 module 3 writes or reads to/from Address 0x3500000 as shown in figure 3 by reference numeral 19. The PLD then performs a determination 21 as to whether the action at memory address 19 is a read or write. If the TMS470 module 3 is performing a write 23, the state machine of the PLD as shown in figure 4 starts, and the necessary control signals are generated 25. The PLD will take all 16 bits of the TMS470 module 3 data bus, latch the lower 8, transfer the high byte to the HPI data bus of the TMS320 module 9, set HBIL signal to high, then transfer the latched lower byte data to the HPI data bus.

If TMS470 module 3 is performing a read 27, the state machine starts and the necessary control signals are generated 29. The PLD will take the data from the HPI data bus, and will latch this data, then set Hbil High, and will then get the other 8 bits from the HPI data bus. The PLD will then place all 16 bits (including the first 8 bits that were latched) to the higher data

bits and the last 8 bits from the HPI to the lower TMS470 module 3 data bits.

While specific embodiments of the invention have been shown and described in detail to illustrate the application of the principles of the invention, it will be understood that the invention may be embodied otherwise without departing from such principles.